1 General Description

The AS5043 is a contactless magnetic angle encoder for accurate measurement up to 360°.

It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

The AS5043 provides a digital 10-bit as well as a programmable analog output that is directly proportional to the angle of a magnet, rotating over the chip.

The analog output can be configured in many ways, including user programmable angular range, adjustable output voltage range, voltage or current output, etc..

An internal voltage regulator allows operation of the AS5043 from 3.3V or 5.0V supplies.

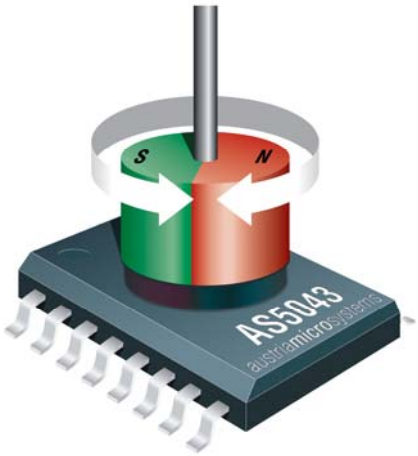


Figure 1: Typical arrangement of AS5043 and magnet

2 Benefits

Complete system-on-chip

- Flexible system solution provides absolute output, both digital and analog
- Angle measurement with software programmable range up to 360°
- High reliability due to non-contact magnetic sensing
- Ideal for applications in harsh environments
- Robust system, tolerant to magnet misalignment, airgap variations, temperature variations and external magnetic fields
- No calibration required

3 Key Features

360° contactless high resolution angular position encoding

User programmable zero position

Two 10-bit absolute outputs:

Serial digital interface and

Versatile analog output
programmable angular range up to 360°
programmable ratiometric output voltage range

Failure detection mode for magnet field strength and loss of power supply

Serial read-out of multiple interconnected AS5043 devices using daisy chain mode

Mode input for optimizing noise vs. speed

Alignment mode for magnet placement guidance

Wide temperature range: - 40°C to + 125°C

Small package: SSOP 16 (5.3mm x 6.2mm)

4 Applications

The AS5043 is ideal for applications with an angular travel range from a few degrees up to a full turn of 360°, such as

- Industrial applications:
  - Contactless rotary position sensing
  - Robotics
  - Valve Controls
- Automotive applications:
  - Throttle position sensors
  - Gas / brake pedal position sensing
  - Headlight position control

Front panel rotary switches

Replacement of potentiometers

5 Pin Configuration

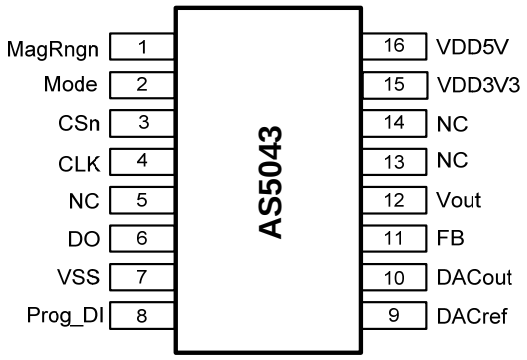


Figure 2: AS5043 pin configuration SSOP16

Package = SSOP16 (16 lead Shrink Small Outline Package)

Pin	Symbol	Type	Description
1	MagRngn	DO_OD	Magnet Field Magnitude RaNGe warning; active low, indicates that the magnetic field strength is outside of the recommended limits.
2	Mode	DI_PD, ST	Mode input. Select between low noise (open, low) and high speed (high) mode. Internal pull-down resistor
3	CSn	DI_PU, ST	Chip Select, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
4	CLK	DI,ST	Clock Input of Synchronous Serial Interface; Schmitt-Trigger input
5	NC	-	must be left unconnected
6	DO	DO_T	Data Output of Synchronous Serial Interface
7	VSS	S	Negative Supply Voltage (GND)
8	Prog_DI	DI_PD	OTP Programming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Should be connected to VSS if programming is not used
9	DACref	AI	DAC Reference voltage input for external reference
10	DACout	AO	DAC output (unbuffered, Ri ~8kΩ)
11	FB	AI	Feedback, OPAMP inverting input
12	Vout	AO	OPAMP output
13	NC	-	Must be left unconnected
14	NC	-	Must be left unconnected
15	VDD3V3	S	3V-Regulator Output for internal core, regulated from VDD5V.Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V

Table 1: Pin description SSOP16

DO_OD	digital output open drain	S	supply pin
DI_PD	digital input pull-down	DO_T	digital output /tri-state
DI_PU	digital input pull-up	ST	schmitt-trigger input
AI	analog input	AO	analog output
DI	digital input		

5.1 Pin Description

Pins 7, 15 and 16 are supply pins, pins 5, 13 and 14 are for internal use and must be left open.

Pin 1 is the magnetic field strength indicator, MagRNGn. It is an open-drain output that is pulled to VSS when the magnetic field is out of the recommended range (45mT to 75mT). The chip will still continue to operate, but with reduced performance, when the magnetic field is out of range. When this pin is low, the analog output at pins #10 and #12 will be 0V to indicate the out-of-range condition.

Pin 2 MODE allows switching between filtered (slow) and unfiltered (fast mode). See section 9.

Pin 3 Chip Select (CSn; active low) selects a device for serial data transmission over the SSI interface. A “logic high” at CSn forces output DO to digital tri-state.

Pin 4 CLK is the clock input for serial data transmission over the SSI interface (see section 8)

Pin 6 DO (Data Out) is the serial data output during data transmission over the SSI interface (see section 8)

Pin 8 PROG_DI is used to program the different operation modes, as well as the zero-position in the OTP register.

This pin is also used as a digital input to shift serial data through the device in Daisy Chain Configuration, (see page 6).

Pin 9 DACref is the external voltage reference input for the Digital-to-Analog Converter (DAC). If selected, the analog output voltage on pin 12 (V_{out}) will be ratiometric to the voltage on this pin.

Pin10 DACout is the unbuffered output of the DAC. This pin may be used to connect an external OPAMP, etc. to the DAC.

Pin 11 FB (Feedback) is the inverting input of the OPAMP buffer stage.

Access to this pin allows various OPAMP configurations.

Pin 12 Vout is the analog output pin. The analog output is a DC voltage, ratiometric to VDD5V (3.0 – 5.5V) or an external voltage source and proportional to the angle.

6 Functional Description

The AS5043 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed in a circle around the center of the device and deliver a voltage representation of the magnetic field perpendicular to the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5043 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used indicate movements of the magnet towards or away from the chip and to indicate, when the magnetic field is outside of the recommended range (status bits = MagInc, MagDec; hardware pin = MagRngn).

A small low cost diametrically magnetized (two-pole) standard magnet, centered over the chip, is used as the input device.

The AS5043 senses the orientation of the magnetic field and calculates a 10-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, the absolute angular representation is converted to an analog signal, ratiometric to the supply voltage.

The analog output can be configured in many ways, such as 360°/180°/90° or 45° angular range, external or internal DAC reference voltage, 0-100%*VDD or 10-90% *VDD analog output range, external or internal amplifier gain setting.

The various output modes as well as a user programmable zero position can be programmed in an OTP register. As long as no programming voltage is applied to pin PROG, the new setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by applying a programming voltage.

The AS5043 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

It is also tolerant to airgap and temperature variations due to Sin-/Cos- signal evaluation.

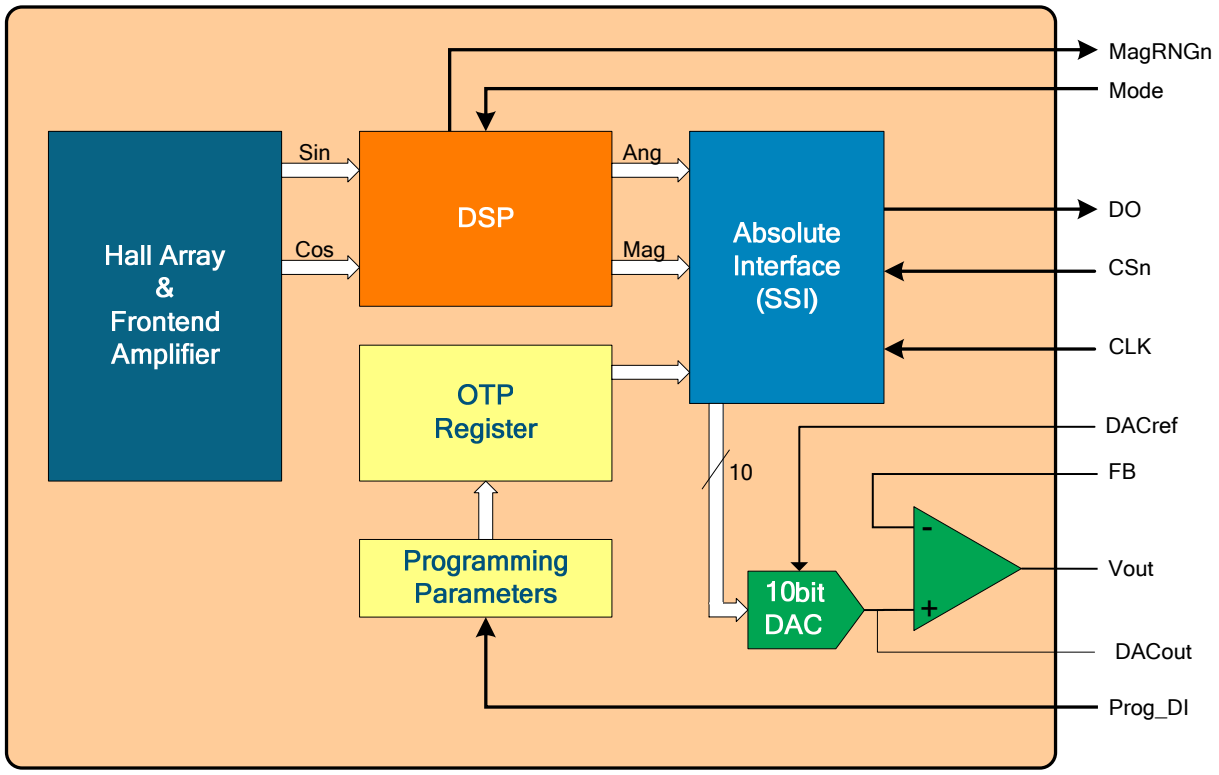


Figure 3: AS5043 block diagram

7 3.3V / 5V Operation

The AS5043 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The core supply voltage is always taken from the LDO output, as the internal blocks are always operating at 3.3V.

For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 4).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10µF capacitor, which should be placed close to the supply pin (see).

The VDD3V3 output is intended for internal use only It should not be loaded with an external load.

The voltage levels of the digital interface I/O's correspond to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin (see Figure 4).

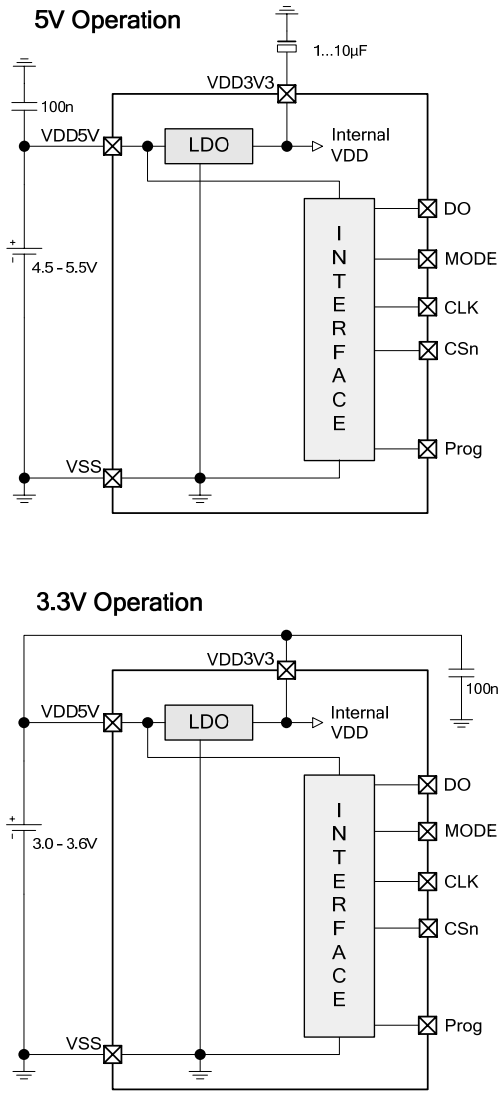


Figure 4: Connections for 5V / 3.3V supply voltages

A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

8 10-bit Absolute Synchronous Serial Interface (SSI)

The serial data transmission timing is outlined in Figure 5: if CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out sequence will be initiated.

After a minimum time $t_{CLK\ FE,}$ data is latched into the output shift register with the first falling edge of CLK.

Each subsequent rising CLK edge shifts out one bit of data.

The serial word contains 16 bits, the first 10 bits are the angular information D[9:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase / decrease / out of range) .

A subsequent measurement is initiated by a logic "high" pulse at CSn with a minimum duration of $t_{CSn.}$

Data transmission may be terminated at any time by pulling CSn = high.

8.1 Serial Data Contents:

D9:D0 absolute angular position data (MSB is clocked out first).

OCF (Offset Compensation Finished), logic high indicates that the Offset Compensation Algorithm has finished and data is valid.

COF (Cordic Overflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value.

This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (Linearity Alarm), logic high indicates that the input field generates a critical output linearity.

When this bit is set, the data at D9:D0 may still be used, but may contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Data D9:D0 is valid, when the status bits have the following configurations:

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	even checksum of bits 1:15
			0	1	
			1	0	

Table 2: Status bit outputs

MagInc, (Magnitude Increase) becomes HIGH, when the magnet is pushed towards the IC, thus the magnetic field strength is increasing.

MagDec, (Magnitude Decrease) becomes HIGH, when the magnet is pulled away from the IC, thus the magnetic field strength is decreasing.

Both signals HIGH indicate a magnetic field that is out of the allowed range (see Table 3).

Note: Pin 1 (MagRngn) is a combination of MagInc and MagDec. It is active low via an open drain output and requires an external pull-up resistor. If the magnetic field is in range, this output is turned off. (logic “high”).

Even Parity bit for transmission error detection of bits 1...15 (D9...D0, OCF, COF, LIN, MagInc, MagDec)

The absolute angular output is always set to a resolution of 10 bit / 360°. Placing the magnet above the chip, angular values increase in clockwise direction by default.

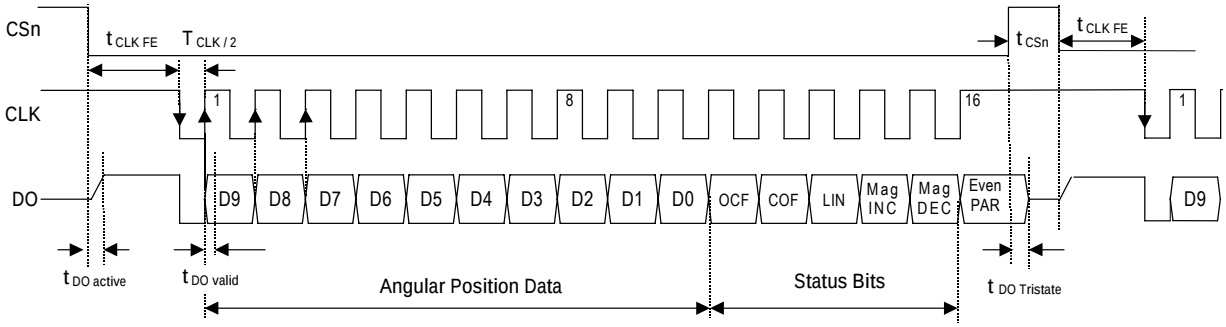


Figure 5: Synchronous serial interface with absolute angular position data

8.2 Z-Axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5043 provides several options of detecting movement and distance of the magnet in the vertical (Z-) direction. Signal indicators MagINC, MagDEC and LIN are available as status bits in the serial data stream, while MagRngn is an open-drain output that indicates an out-of range status (on in YELLOW or RED range). Additionally, the analog output provides a safety feature in the form that it will be turned off when the magnetic field is too strong or too weak (RED range). The serial data is always available, the red/yellow/green status is indicated by the status bits as shown below:

SSI Status bits			Hardware Pins		Description
Mag INC	Mag DEC	LIN	Mag Rngn	Analog output	
0	0	0	Off	enabled	No distance change Magnetic Input Field OK (GREEN range, ~45...75mT)
0	1	0	Off	enabled	Distance increase, GREEN range; Pull-function. This state is dynamic and only active while the magnet is moving away from the chip.
1	0	0	Off	enabled	Distance decrease, GREEN range; Push- function. This state is dynamic and only active while the magnet is moving towards the chip.
1	1	0	On	enabled	YELLOW Range: Magnetic field is ~ 25...45mT or ~75...135mT. The AS5043 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	disabled	RED Range: Magnetic field is ~<25mT or >~135mT. The analog output will be turned off in this range by default. It can be enabled permanently by OTP programming (see 11.1.2). It is still possible to use the absolute serial interface in the red range, but not recommended.

Table 3: Magnetic field strength indicators

9 Mode Input Pin

The absolute angular position is sampled at a rate of 10.4kHz (t=96µs) in fast mode and at a rate of 2.6kHz (t=384µs) in slow mode.

These modes are selected by pin MODE (#2). The mode input pin activates or deactivates an internal filter, which is used to reduce the digital jitter and consequently the analog output noise.

Activating the filter by pulling Mode = LOW or leaving it open reduces the transition noise to <0.03° rms. At the same time, the sampling rate is reduced to 2.6kHz and the signal propagation delay is increased to 384µs. This mode is recommended for high precision, low speed and ≤360° applications.

Deactivating the filter by setting Mode = HIGH increases the sampling rate to 10.4kHz and reduces the signal propagation delay to 96µs. The transition noise will increase to <0.06° rms. This mode is recommended for higher speed and full scale = 360° applications.

Switching the MODE pin affects the following parameters:

Parameter	slow mode (Pin MODE = 0 or open)	fast mode (Pin MODE = 1)
sampling rate	2.61 kHz (383µs)	10.42 kHz (95.9µs)
transition noise (1 sigma)	≤ 0.03° rms	≤ 0.06° rms
propagation delay	384µs	96µs
Startup time	20ms	80ms

Table 4: Mode pin settings

Pin MODE should be set at power-up. A mode change during operation is not recommended.

10 Daisy Chain Mode

The Daisy Chain Mode allows connection of several AS5043's in series, while still keeping just one digital input for data transfer (See "Data IN" in Figure 6). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PROG; pin 8) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is

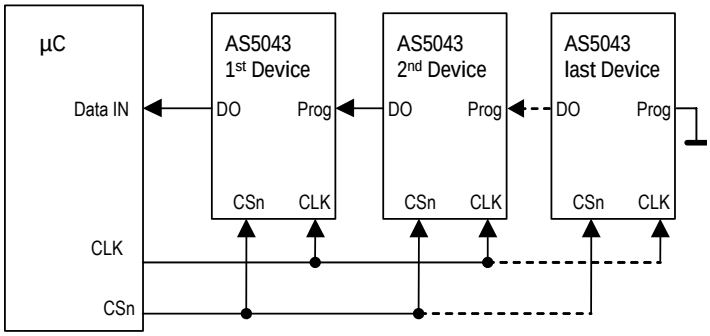


Figure 6: Daisy Chain hardware configuration

n * (16+1) bits:

e.g. 34 bit for two devices, 51 bit for three devices, etc...

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D9), etc... (see Figure 7)

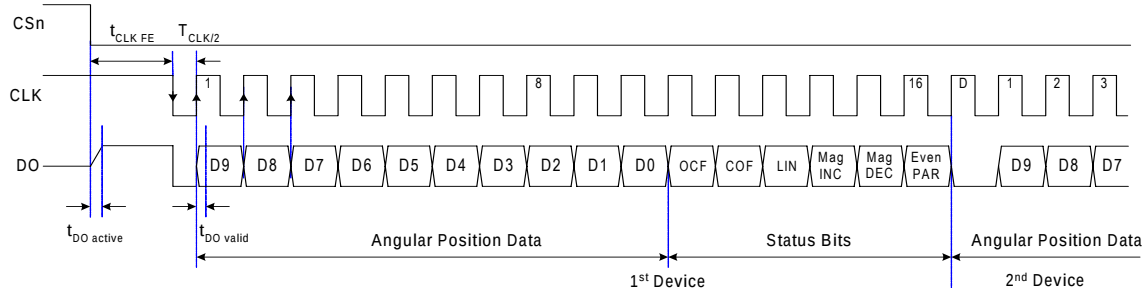


Figure 7: Daisy Chain data transfer timing diagram

11 Analog Output

The analog output V_{out} provides an analog voltage that is proportional to the angle of the rotating magnet and ratiometric to the supply voltage VDD5V (max.5.5V). It can source or sink currents up to ±1mA in normal operation (up to 66mA short circuit current).

The analog output block consists of a digital angular range selector, a 10-bit Digital-to-Analog converter and an OPAMP buffer stage (see Figure 14).

The digital range selector allows a preselection of the angular range for 360°,180°,90° or 45° (see Table 5). Fine-tuning of the angular range can be accomplished by adjusting the gain of the OPAMP buffer stage.

The reference voltage for the Digital-to-Analog converter (DAC) can be taken internally from VDD5V / 2. In this mode, the output voltage is ratiometric to the supply voltage.

Alternatively, an external DAC reference can be applied at pin DACref (#9). In this mode, the analog output is ratiometric to the external reference voltage.

An on-chip diagnostic feature turns the analog output off in case of an error (broken supply or magnetic field out of range; see Table 3).

The DAC output can be accessed directly at pin #10 DACout.

The addition of an OPAMP to the DAC output allows a variety of user configurable options, such as variable output voltage ranges and variable output voltage versus angle response. By adding an external transistor, the analog voltage output can be buffered to allow output currents up to hundred milliamperes or more.

Furthermore, the OPAMP can be configured as constant current source.

As an OTP option, the DAC can be configured to 2 different output ranges:

a) 0……100% V_{DACref}. The reference point may be either taken from VDD5V/2 or from the external DACref input. The 0...100% range allows easy replacement of potentiometers. Due to the nature of rail-to-rail outputs, the linearity will degrade at output voltages that are close to the supply rails.

b) 10…..90% V_{DACref}. This range allows better linearity, as the OPAMP is not driven to the rails. Furthermore, this mode allows failure detection, when the analog output voltage is outside of the normal operating range of 10...90%VDD, as in the case of broken supply or when the magnetic field is out of range and the analog output is turned off.

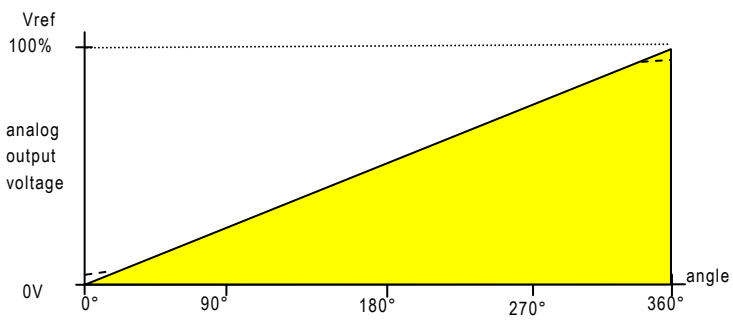
11.1 Analog output voltage modes

The Analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be selected as rail-to-rail output or as clamped output with 10%-90% VDD5V.

The output is ratiometric to the supply voltage (VDD5V), which can range from 3.0V to 5.5V. If the DAC reference is switched to an external reference (pin DACref), the output is ratiometric to the external reference.

11.1.1 Full Scale Mode

This output mode provides a ratiometric DAC output of (0% to 100%)x Vref *), amplified by the OPAMP stage (default = internal 2x gain, see Figure 14)

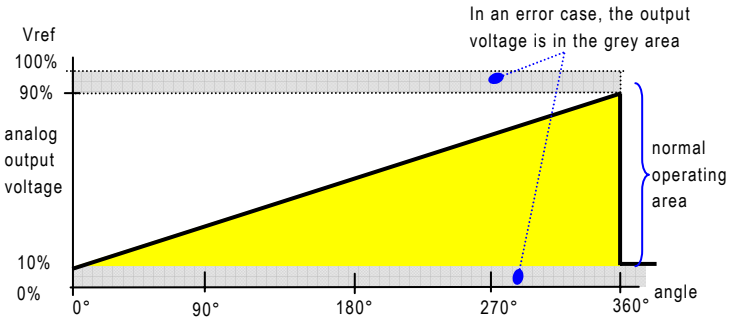


Note: For simplification, Figure 8 describes a linear output voltage from rail to rail (0V to VDD). In practice, this is not feasible due to saturation effects of the OPAMP output driver transistors. The actual curve will be rounded towards the supply rails (as indicated in Figure 8).

Figure 8: Analog output, full scale mode (shown for 360°mode)

Note: Figure 8 and are shown for 360° operation. See Table 5 (page 12) for further angular range programming options.

11.1.2 Diagnostic Output Mode



In Diagnostic Output Mode (see Figure 9) the analog output of the internal DAC ranges from 10% - 90% Vref*). In an error case, either when the supply is interrupted or when the magnetic field is in the "red" range, (see Table 3) the output is switched to 0V and thus indicates the error condition.

Figure 9: Diagnostic Output Mode

It is possible to enable the analog output permanently (it will not be switched off even if the magnetic field is out of range). To enable this feature an OTP bit in the factory setting must be set. The corresponding bit is FS6. See application note AS5040-20 (Extended features of OTP programming) for further details. The application note is available for download at the austriamicrosystems website.

The analog and digital outputs will have the following conditions:

Status	DAC output voltage	SSI digital output
normal operation	10% - 90% Vref*)	#0 - #1023 (0°-360°), MagRngn = 1
magnetic field out of range	< 10% Vref*), DAC output is switched to 0V	#0 - #1023 (0°-360°) out of range is signaled in status bits: MagInc=MagDec=LIN=1, MagRngn= 0
broken positive power supply (V_{OUT} pull down resistor at receiving side)	< 10% VDD**)	with pull down resistor at DO (receiving side), all bits read by the SSI will be "0"-s, indicating a non-valid output
broken power supply ground (V_{OUT} pull down resistor at receiving side)	< 10% VDD**)	
broken positive power supply (V_{OUT} pull up resistor at receiving side)	> 90% VDD**)	
broken power supply ground (V_{OUT} pull up resistor at receiving side)	> 90% VDD**)	

*) Vref = internal: ½ * VDD5V (pin #16) or external: V_{DACref} (pin#9), depending on Ref_extEN bit in OTP (0=int., 1=ext.)

**) VDD = positive supply voltage at receiving side (3.0 – 5.5V)

12 Programming the AS5043

After power-on, programming the AS5043 is enabled with the rising edge of CSn and Prog = logic high. 16 bit configuration data must be serially shifted into the OTP register via the Prog-pin. The first "CCW" bit is followed by the zero position data (MSB first) and the Analog Output Mode setting as shown in Table 5. Data must be valid at the rising edge of CLK (see Figure 10). Following this sequence, the voltage at pin Prog must be raised to the programming voltage V_{PROG} (see Figure 11). 16 CLK pulses (t_{PROG}) must be applied to program the fuses. To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

Note: During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals PROG and VSS must be kept as short as possible. The maximum wire length between the V_{PROG} switching transistor and pin PROG (Figure 12) should not exceed 50mm (2 inches).

To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins PROG and VSS. This capacitor is only required for programming, it is not required for normal operation. The clock timing t_{clk} must be selected at a proper rate to ensure that the signal PROG is stable at the rising edge of CLK (see Figure 10). Additionally, the programming supply voltage should be buffered with a 10µF capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming. The specified programming voltage at pin PROG is 7.3 – 7.5V (see section 19.7). To compensate for the voltage drop across the V_{PROG} switching transistor, the applied programming voltage may be set slightly higher (7.5 - 8.0V, see Figure 12).

OTP Register Contents:

CCW Counter Clockwise Bit

ccw=0 – angular value increases with clockwise rotation

ccw=1 – angular value increases with counterclockwise rotation

Z [9:0]: Programmable Zero / Index Position

FB_intEN: OPAMP gain setting: 0=external, 1=internal

RefExtEN: DAC reference: 0=internal, 1=external

ClampMd EN: Analog output span: 0=0-100%, 1=10-90%*VDD

Output Range (OR0, OR1):

	Analog Output Range Selection	
[1:0]	00 = 360°	01 = 180°
	10 = 90°	11 = 45°

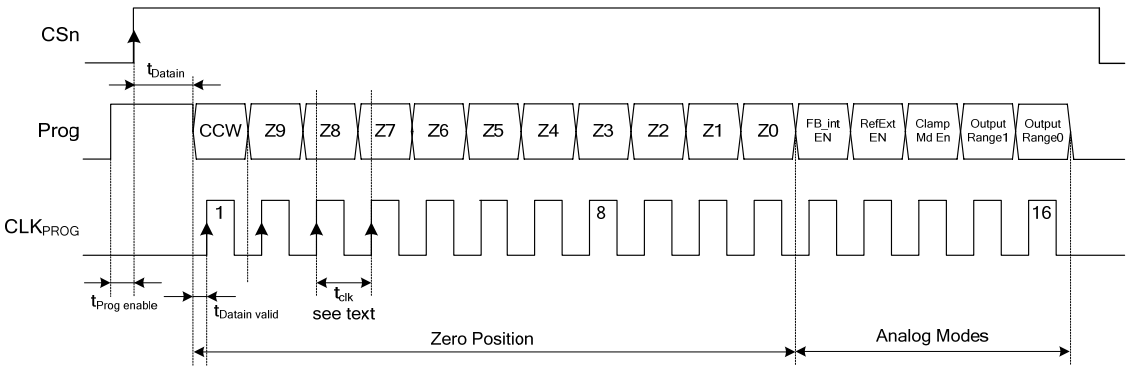


Figure 10: Programming Access – OTP Write Cycle (section of Figure 11)

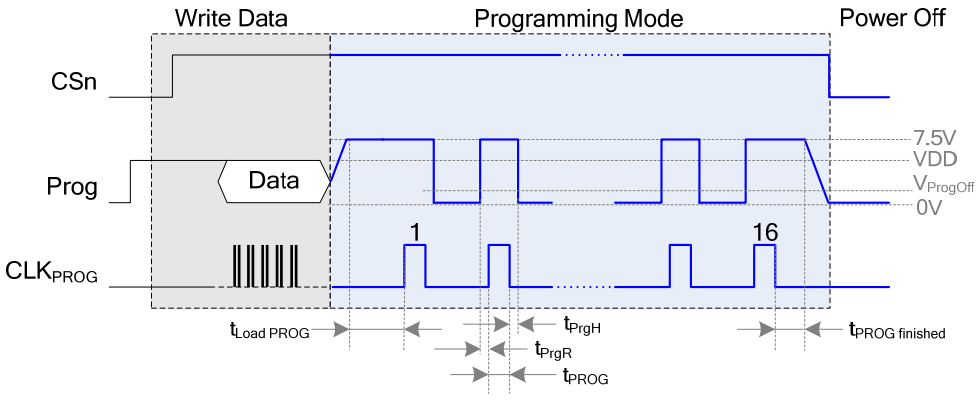


Figure 11: Complete OTP programming sequence

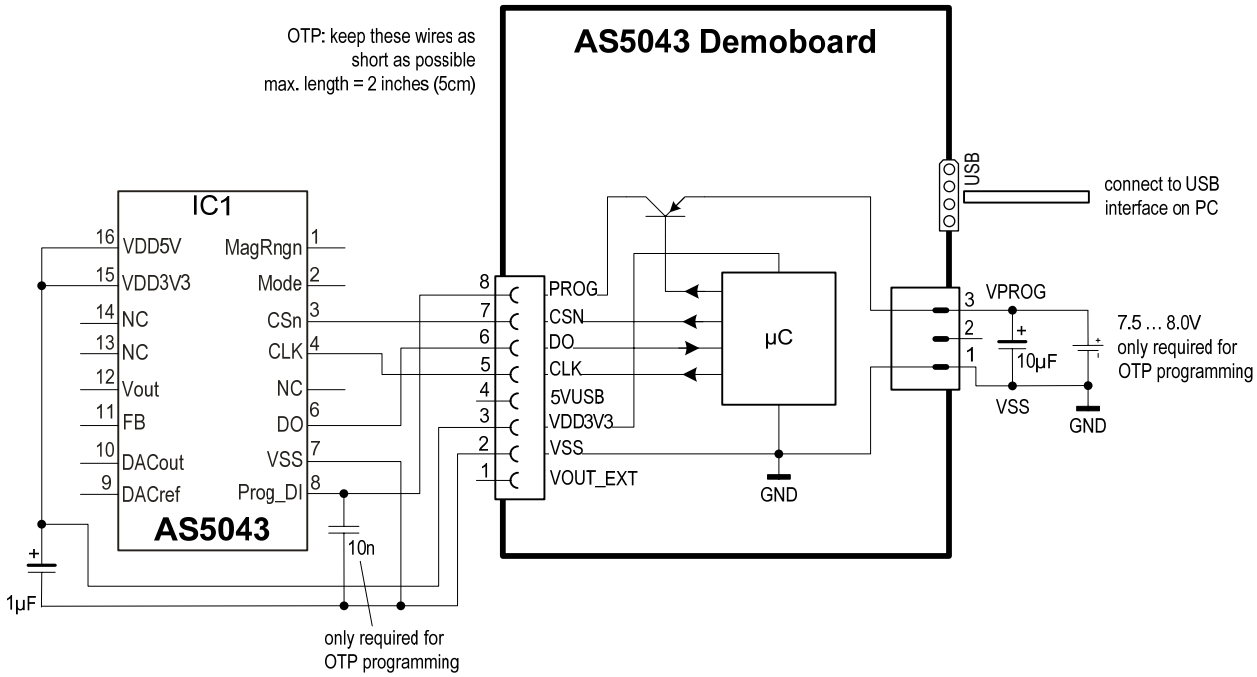


Figure 12: OTP programming hardware connection of AS5043 (shown with AS5043 demoboard)

12.1 Zero Position Programming

The AS5043 allows easy assembly of the system, as the actual angle of the magnet does not need to be considered. By OTP programming, any position can be assigned as the new permanent zero position with an accuracy of 0.35° (all modes).

Using the same procedure, the AS5043 can be calibrated to assign a given output voltage to a given angle. With this approach, all offset errors (DAC + OPAMP) are also compensated for the calibrated position.

Essentially, for a given mechanical position, the angular measurement system is electrically rotated (by changing the Zero Position value in the OTP register), until the output matches the desired mechanical position.

The example in Figure 13 below shows a configuration for 5V supply voltage and 10%-90% output voltage range. It adjusted by Zero Position Programming to provide an analog output voltage of 2.0 Volts at an angle of 180°. The slope of the curve may be further adjusted by changing the gain of the OPAMP output stage and by selecting the desired angular range (360°/180°/90°/45°).

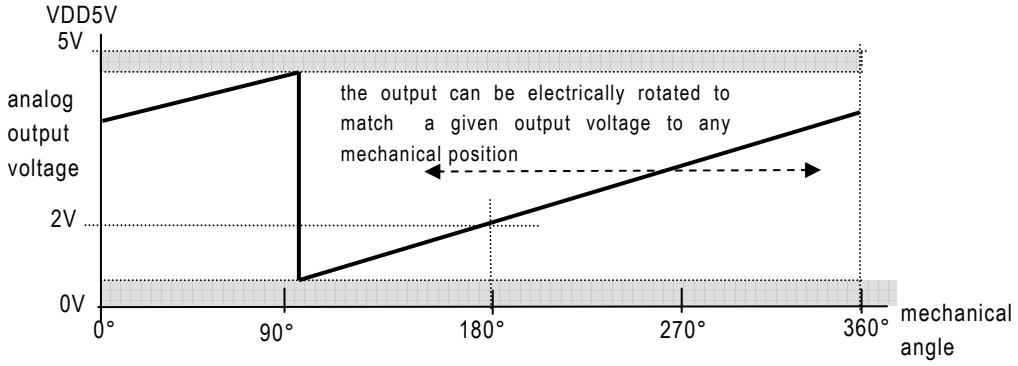


Figure 13: Zero position programming (shown for 360° mode)

12.2 Analog Mode Programming

The analog output can be configured in many ways:

It consists of three major building blocks,

a digital range preselector,

a 10-bit Digital-to-Analog-Converter (DAC)

and an OP-AMP buffer stage.

In the default configuration (all OTP bits = 0), the analog output is set for 360° operation, internal DAC reference (VDD5V/2), external OPAMP gain, 0-100% ratiometric to VDD5V.

Shown below is a typical example for a 0°-360° range, 0-5V output. The complete application requires only one external component, a buffer capacitor at VDD3V3 and has only 3 connections VDD, VSS and Vout (connectors 1-3).

Note: the default setting for the OPAMP feedback path is:FB_intEn=0=external. The external resistors Rf and Rg must be installed. In the programmed state (FB_intEn=1=internal), these resistors do not need to be installed as the feedback path is internal (Rf_int and Rg_int).

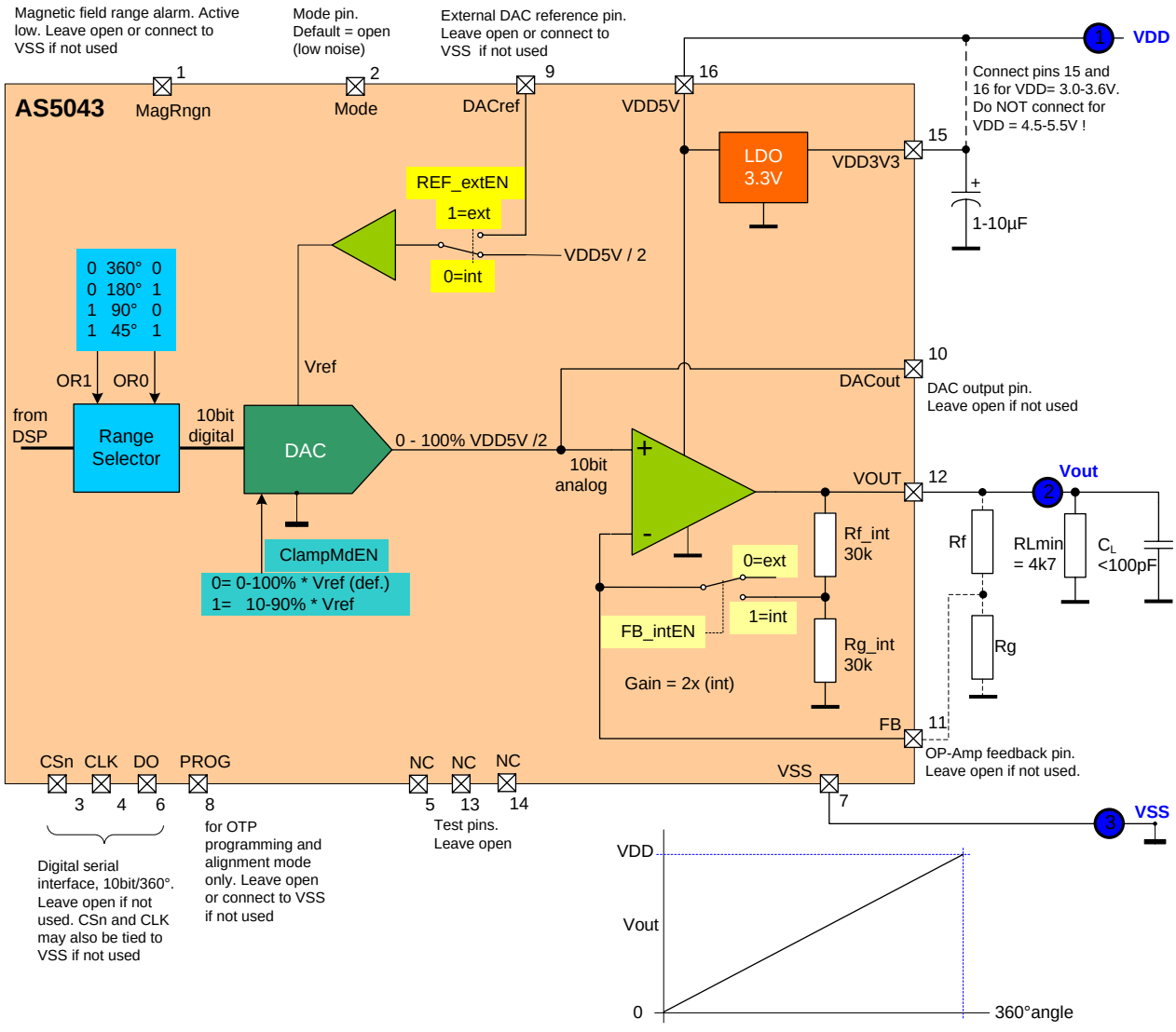


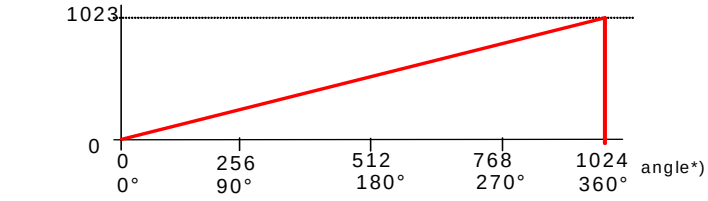
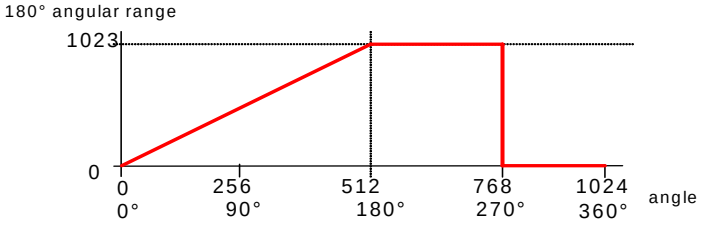
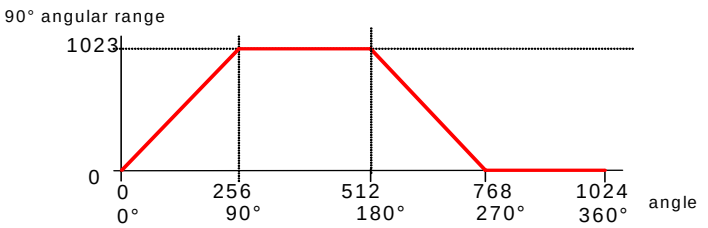
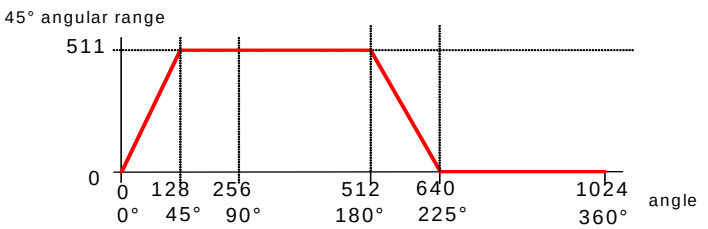
Figure 14: analog output block diagram

12.2.1 Angular range Selector :

The Angular Range selector allows a digital pre-selection of the angular range. The AS5043 can be configured for a full scale angular range of 45°,90°,180° or 360°. In addition, the Output voltage versus angle response can be fine-tuned by setting the gain of the OP-AMP with external resistors and the maximum output voltage can be set in the DAC.

The combination of these options allows to configure the operation range of the AS5043 for all angles up to 360° and output voltages up to 5.5V

The response curve for the analog output is linear for the selected range (45°/90°/180°/360°). In addition, the slope is mirrored at 180° for 45°- and 90°- modes and has a step response at 270° for the 180°-mode. This allows the AS5043 to be used in a variety of applications. In these three modes, the output remains at $V_{out,max}$ and $V_{out,min}$ to avoid a sudden output change when the mechanical angle is rotated beyond the selected analog range. In 360°-mode, a jitter between $V_{out,max}$ and $V_{out,min}$ at the 360° point is also prevented due to a hysteresis.

Output Range1	Output Range0	Mode	Note
0	0	360° angular range (default) 	default mode, analog resolution= 10bit (1024 steps) over 360° analog step size: 1LSB = 0.35°
0	1	180° angular range 	analog resolution= 10bit (1024 steps) over 180° Analog step size: 1LSB = 0.175°
1	0	90° angular range 	analog resolution= 10bit (1024 steps) over 90° Analog step size: 1LSB = 0.088°
1	1	45° angular range 	analog resolution= 9 bit (512 steps) over 45° Analog step size: 1LSB = 0.088°

**) Note: the resolution on the digital SSI interface is always 10bit (0.35°/step) over 360°, independent on analog mode*

Table 5: Digital Range Selector programming option

12.3 Repeated OTP Programming

Although a single AS5043 OTP register bit can be programmed only once (from 0 to 1), it is possible to program other, unprogrammed bits in subsequent programming cycles. However, a bit that has already been programmed should not be programmed twice. Therefore it is recommended that bits that are already programmed are set to “0” during a programming cycle.

12.4 Non-permanent Programming

It is also possible to re-configure the AS5043 in a non-permanent way by overwriting the OTP register.

This procedure is essentially a “Write Data” sequence (see Figure 10) without a subsequent OTP programming cycle.

The “Write Data” sequence may be applied at any time during normal operation. This configuration remains set while the power supply voltage is above the power-on reset level (see 19.5).

See Application Note AN5000-20 for further information.

12.5 Digital-to-Analog Converter (DAC)

The DAC has a resolution of 10bit (1024 steps) and can be configured for the following options

Internal or external reference

The default DAC reference is the voltage at pin #16 (VDD5V) divided by 2 (see Figure 14). Using this reference, a system that has an output voltage ratiometric to the supply voltage can be built.

Optionally, an external reference source, applied at pin#9 (DACref) can be used. This programming option is useful for applications requiring a precise output voltage that is independent of supply fluctuations, for current sink outputs or for applications with a dynamic reference, e.g. attenuation of audio signals.

0-100% or 10-90% full scale range

The reference voltage for the DAC is buffered internally. The recommended range for the external reference voltage is 0.2V to (VDD3V3 -0.2)V.

The DAC output voltage will be switched to 0V, when the magnetic field is out of range, when the MagInc and MagDec indicators are both =1 and the MagRngn-pin (#1) will go low.

The default full scale output voltage range is 0-100%*VDD5V. Due to limitations in the output stage of an OP-Amp buffer, it cannot drive the output voltage from 0-100% rail-to-rail. Without load, the minimum output voltage at 0° will be a few millivolts higher than 0V and the maximum output voltage will be slightly lower than VDD5V . With increasing load, the voltage drops will increase accordingly.

As a programming option, an output range of 10-90%*VDD5V can be selected. In this mode, there is no saturation at the upper and lower output voltage limits like in the 0-100% mode and it allows failure detection as the output voltage will be outside the 10-90% limits, when the magnetic field is in the “red” range (V_{out}=0V, see Table 3) or when the supply to the chip is interrupted (V_{out}=0V or VDD5V).

The unbuffered output of the DAC is accessible at pin #10 (DACout). This output must not be loaded.

12.6 OP-AMP stage

The DAC output is buffered by a non-inverting Op-Amp stage. The amplifier is supplied by VDD5V (pin #16) and can hence provide output voltages up to 5V.

By allowing access to the inverting input of the Op-Amp and with the addition of a few discrete components it can be configured in many ways, like high current buffer, current sink output, adjustable angle range, etc...

Per default, the gain of the Op-Amp must be set by two external resistors (see Figure 14). Optionally, the fixed internal gain setting (2x) may be programmed by OTP, eliminating the need for external resistors.

12.6.1 Output Noise

The Noise level at the analog output depends on two states of the digital angular output:

a) the digital angular output value is stable
In this case, the output noise is the figure given as V_{noise} in paragraph 19.3.6. Note that the noise level is given for the default gain of 2x For other gains, it must be scaled accordingly.

b) the digital output is at the edge of a step
In this case, the digital output may jitter between two adjacent values. The rate of jitter is specified as transition noise (parameter TN in paragraph 19.5). The resulting output noise is calculated by:

$$V_{noise,Vout} = \frac{TN * VDD5V}{360} + V_{noise,OPAMP}$$

where:

$V_{noise, Vout}$	= noise level at pin Vout in Vrms
TN	= transition noise (in °rms; see 19.5)
VDD5V	= Supply voltage VDD5V in V
$V_{noise,OPAMP}$	= noise level of OPAMP (paragraph 19.3.6) in Vrms

12.7 Application Examples

See Application Note AN5043-10 for AS5043 Application Examples.

13 Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bits, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5043 in Analog Readback Mode, a digital sequence must be applied to pins CSn, PROG and CLK as shown in Figure 15. The digital level for this pin depends on the supply configuration (3.3V or 5V; see section 7, page 4).

The second rising edge on CSn (OutpEN) changes pin PROG to a digital output and the log. high signal at pin PROG must be removed to avoid collision of outputs (grey area in Figure 15).

The following falling slope of CSn changes pin PROG to an analog output, providing a reference voltage V_{ref}, that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits.

Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming. (see Figure 15: Output Range OR0 and -1 , ClampMdEn, RefExtEn, FB_IntEn, Z0...Z9, ccw)

During analog readback, the capacitor at pin PROG (see Figure 12) should be removed to allow a fast readout rate.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref}, and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up.

Following the 16th clock (after reading bit “ccw”), the chip must be reset by disconnecting the power supply.

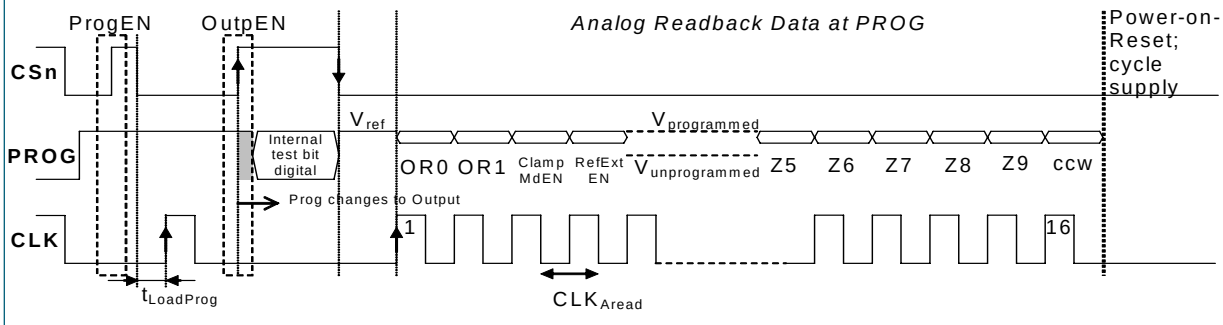


Figure 15:Analog OTP Register Read

14 Alignment Mode

The alignment mode simplifies centering the magnet over the chip to gain maximum accuracy and XY-alignment tolerance.

This electrical centering method allows a wider XY-alignment tolerance (0.485mm radius) than mechanical centering (0.25mm radius) as it eliminates the placement tolerance of the die within the IC package (+/- 0.235mm).

Alignment mode can be enabled with the falling edge of CSn while PROG = logic high (Figure 16). The Data bits D9-D0 of the SSI change to a 10-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 32 over a full turn.

Stronger magnets or short gaps between magnet and IC may show values larger than 32. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The MagInc and MagDec indicators will be = 1 when the alignment mode reading is < 32. At the same time, hardware pin MagRngn (#1) will be pulled to VSS.

The Alignment mode can be reset to normal operation mode by a power-on-reset (cycle power supply) or by a falling edge of CSn with PROG=low (see Figure 17).

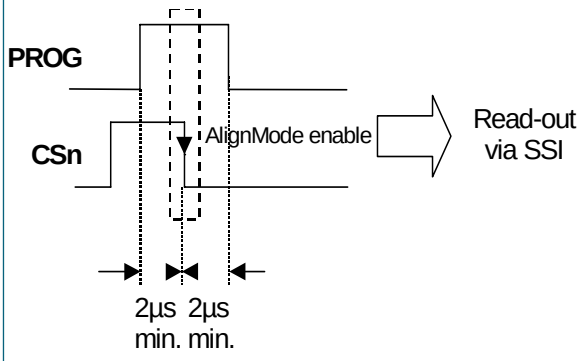


Figure 16: Enabling the alignment mode

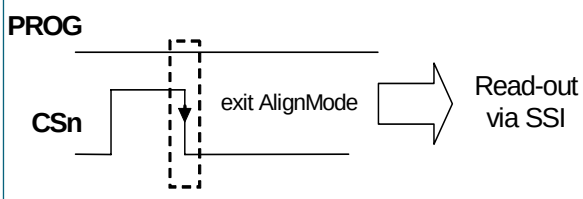


Figure 17:Exiting alignment mode

15 Choosing the proper Magnet

Typically the magnet should be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo, SmCo5 or NdFeB are recommended.

The magnet's field strength perpendicular to the die surface should be verified using a gauss-meter. The magnetic field B_V at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT...±75mT. (see Figure 18).

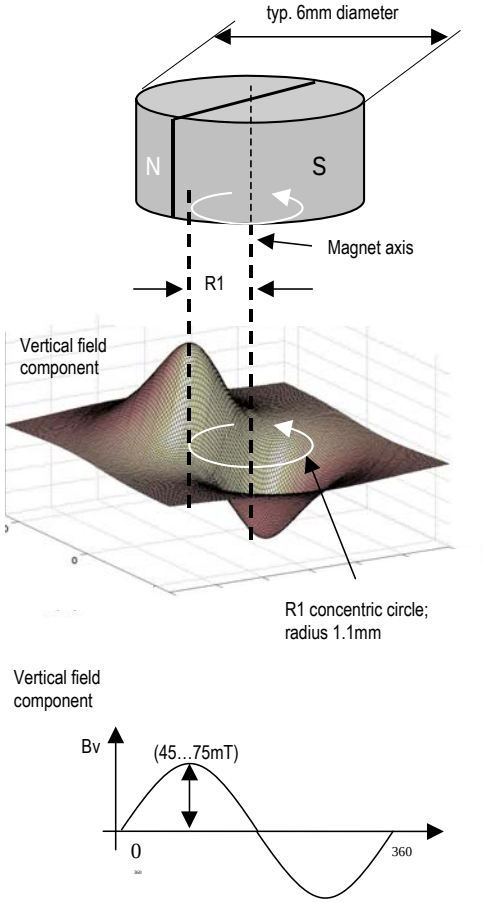


Figure 18: Typical magnet and magnetic field distribution

15.1 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 19:

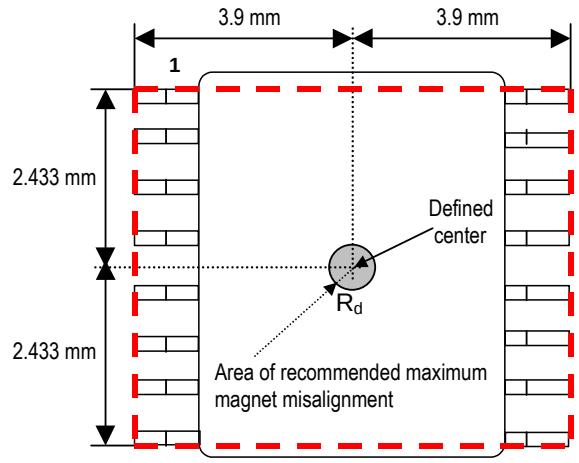


Figure 19: Defined IC center and magnet displacement radius

15.1.1 Magnet Placement:

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC with reference to the edge of pin #1 (see Figure 19). This radius includes the placement tolerance of the chip within the SSOP-16 package (+/- 0.235mm).

The displacement radius R_d is 0.485mm with reference to the center of the chip (see section 14: Alignment Mode).

The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 18). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 3mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits.

A magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagRngn (pin 1), which will be pulled low. At this condition, the angular data is still available over the digital serial interface (SSI), but the analog output will be turned off.

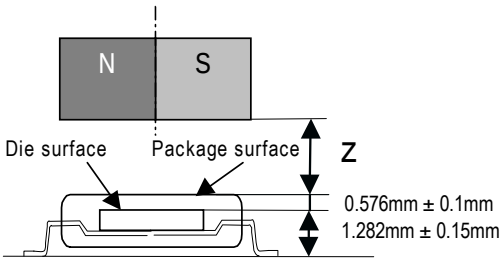


Figure 20: Vertical placement of the magnet

16 Simulation Modelling

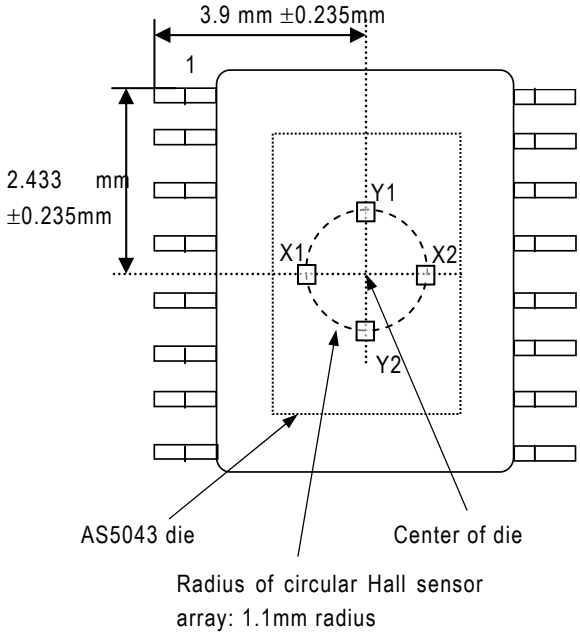


Figure 21: Arrangement of Hall sensor array on chip (principle)

With reference to Figure 21, a diametrically magnetized permanent magnet is placed above or below the surface of the AS5043. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially.

The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field.

The angular displacement (Θ) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$\Theta = \arctan\frac{(Y1-Y2)}{(X1-X2)} \pm 0.5°$$

The ±0.5° angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5043. Placement tolerances of the die within the package are ±0.235mm in X and Y direction, using a reference point of the edge of pin #1 (Figure 21)

In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented.

The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

The recommended differential input range of the magnetic field strength ($B_{(X1-X2)}$,$B_{(Y1-Y2)}$) is ±75mT at the surface of the die. In addition to this range, an additional offset of ±5mT, caused by unwanted external stray fields is allowed.

The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

17 Failure Diagnostics

The AS5043 also offers several diagnostic and failure detection features:

17.1 Magnetic field strength diagnosis

By software: the MagInc and MagDec status bits will both be high when the magnetic field is out of range.

By hardware: Pin #1 (MagRngn) is a logical NAND-ed combination of the MagInc and MagDec status bits. It is an open-drain output and will be turned on (= low with external pull-up resistor) when the magnetic field is out of range.

By hardware: Pin #12 (Vout) is the analog output of the DAC and OP-Amp. The analog output will be 0V, when the magnetic field is out of range (all analog modes).

17.2 Power supply failure detection

By software: If the power supply to the AS5043 is interrupted, the digital data read by the SSI will be all “0”s. Data is only valid, when bit OCF is high, hence a data stream with all “0”s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DO and VSS at the receiving side

By hardware: The MagRngn pin is an open drain output and requires an external pull-up resistor. In normal operation, this pin is high ohmic and the output is high. In a failure case, either when the magnetic field is out of range or the power supply is missing, this output will become low. To ensure an adequate low level in case of a broken power supply to the AS5043, the pull-up resistor (~10kΩ) must be connected to the positive supply at pin 16 (VDD5V).

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18 Angular Output tolerances

18.1 Accuracy; digital outputs

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- the non-linearity of the analog-digital converters,
- internal gain and mismatch errors,
- non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = (Err_{max} – Err_{min})/2 is specified as better than ±0.5 degrees @ 25°C (see Figure 23).

Misalignment of the magnet further reduces the accuracy. Figure 22 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

For each misalignment step, the measurement as shown in Figure 23 is repeated and the accuracy

(Err_{max} – Err_{min})/2 (e.g. 0.25° in Figure 23) is entered as the Z-axis in the 3D-graph.

18.2 Accuracy; analog output

The analog output has the same accuracy as the digital output with the addition of the nonlinearities of the DAC and the OPAMP (+/-1LSB; see Table 5 and 19.3.5).

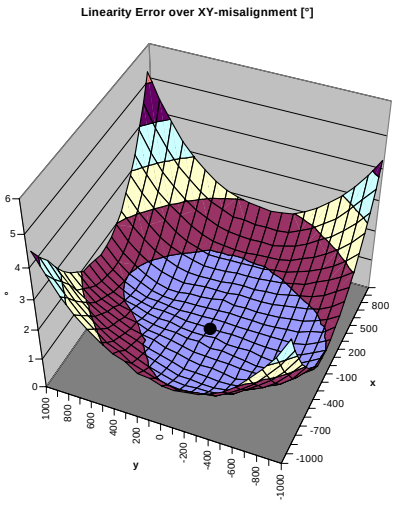


Figure 22: Example of linearity error over XY misalignment

The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees.

The magnet used for these measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

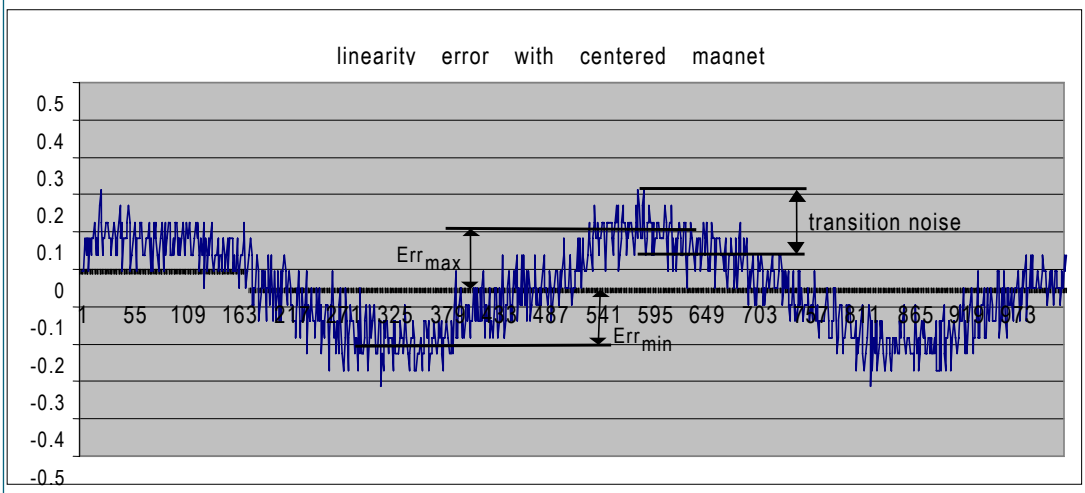


Figure 23: Example of linearity error over 360°

18.3 Transition Noise

Transition noise is defined as the jitter in the transition between two steps.

Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved.

This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)*1 in fast mode (pin MODE = high) and 0.03 degrees rms (1 sigma)*1 in slow mode (pin MODE = low or open).

These values are the repeatability of an indicated angle at a given mechanical position.

The transition noise has different implications on the type of output that is used:

- absolute output; SSI interface:
  The transition noise of the absolute output can be reduced by the user by applying an averaging of readings. An averaging of 4 readings will reduce the transition noise by 6dB or 50%, e.g. from 0.03°rms to 0.015°rms (1 sigma) in slow mode
- analog output:
  Ideally, the analog output should have a jitter that is less than one digit. In 360° mode, both fast or slow mode may be selected for adequate low jitter.
  In 180°, 90° or 45° mode, where the step sizes are smaller, slow mode should be selected to reduce the output jitter.

*1: statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.

18.4 High Speed Operation

18.4.1 Sampling rate

The AS5043 samples the angular value at a rate of 10.42k samples per second (ksps) in fast mode and 2.61ksps in slow mode.

Consequently, a new reading is performed each 96µs. (fast mode) or 384µs (slow mode).

At a stationary position of the magnet, this sampling rate creates no additional error.

Absolute Mode:

With the given sampling rates, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by

$$n = \frac{60}{rpm \cdot 96\mu s}$$ for fast mode

$$n = \frac{60}{rpm \cdot 384\mu s}$$ for slow mode

In practice, there is no upper speed limit. The only restriction is that there will be fewer samples per revolution as the speed increases.

Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution.

Fast Mode (pin Mode = 1)	Slow Mode (pin Mode = 0 or open)
610rpm = 1024 samples / turn	610rpm = 256 samples / turn
1220rpm = 512 samples / turn	1220rpm = 128 samples / turn
2441rpm = 256 samples / turn	2441rpm = 64 samples / turn
etc...	etc...

Table 6: Speed performance

18.5 Output delays

The propagation delay is the delay between the time that the sample is taken until it is available as angular data. This delay is 96µs in fast mode (pin Mode = high) and 384µs in slow mode (pin Mode = low or open)

The analog output produces no further delay, the output voltage will be updated as soon as it is available. Using the SSI interface for data transmission, an additional delay must be considered, caused by the asynchronous sampling (0....1/f_{sample}) and the time it takes the external control unit to read and process the angular data from the AS5043.

18.5.1 Angular error caused by propagation delay

A rotating magnet will cause an angular error caused by the propagation delay.

This error increases linearly with speed:

$$e_{sampling}(\deg) = 6 * rpm * pr.delay$$

where $e_{sampling}$ = angular error [°]
rpm = rotating speed [rpm]
prop.delay = propagation delay [seconds]

Note: since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5043.

Internal timing tolerance

The AS5043 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5043 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to ±5% accuracy at room temperature (±10% over full temperature range). This tolerance influences the ADC sampling rate:

18.5.2 absolute output; SSI interface:

A new angular value is updated every

96µs +/- 5% (Mode = 1) or

384µs +/- 5% (Mode = 0 or open)

18.6 Temperature

18.6.1 Magnetic temperature coefficient

One of the major benefits of the AS5043 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5043 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5043 operates with magnetic field strengths from ±45...±75mT.

Example:
A NdFeB magnet has a field strength of 75mT @ –40°C and a temperature coefficient of -0.12% per Kelvin. The temperature change is from –40° to +125° = 165K.

The magnetic field change is: 165 x -0.12% = -19.8%, which corresponds to 75mT at –40°C and 60mT at 125°C .

The AS5043 can compensate for this temperature related field strength change automatically, no user adjustment is required.

18.6.2 Accuracy over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is ≤ ±0.5° at room temperature, it may increase to ≤±0.9° due to increasing noise at high temperatures.

18.6.3 Timing tolerance over temperature

The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.

19 Electrical Characteristics

19.1 Absolute Maximum Ratings (non operating)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage	VDD5V	-0.3	7	V	Pin VDD5V
	VDD3V3		5	V	Pin VDD3V3
Input pin voltage	V_{in}	-0.3	VDD5V +0.3	V	Pins MagRngn, Mode, CSn, CLK, DO, DACout, FB, Vout
		-0.3	5		Pin DACref
		-0.3	7.5		Pin PROG_DI
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD		± 2	kV	Norm: MIL 883 E method 3015
Storage temperature	T_{strg}	-55	125	°C	Min – 67°F ; Max +257°F
Body temperature (Lead-free package)	T_{Body}		260	°C	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn "matte tin"
Humidity non-condensing	H	5	85	%	

19.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	T_{amb}	-40		125	°C	-40°F…+257°F
Supply current	I_{supp}		16	21	mA	
Supply voltage at pin VDD5V	VDD5V	4.5	5.0	5.5	V	5V Operation
Voltage regulator output voltage at pin VDD3V3	VDD3V3	3.0	3.3	3.6	V	
Supply voltage at pin VDD5V	VDD5V	3.0	3.3	3.6	V	3.3V Operation (pin VDD5V and VDD3V3 connected)
Supply voltage at pin VDD3V3	VDD3V3	3.0	3.3	3.6	V	

19.3 DC Characteristics for Digital Inputs and Outputs

19.3.1 CMOS Schmitt-Trigger Inputs: CLK, CSn (internal Pull-up), Mode (internal Pull-down)

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDD5V		V	Normal operation
Low level input voltage	V_{IL}		0.3 * VDD5V	V	
Schmitt Trigger hysteresis	V_{Ion}- V_{Ioff}	1		V	
Input leakage current	I_{LEAK}	-1	1	µA	Pin CLK, VDD5V = 5.0V
Pull-up low level input current	I_{iL}	-30	-100		Pin CSn, VDD5V= 5.0V
Pull-down high level input current	I_{iH}	30	100		Pin Mode, VDD5V= 5.0V

19.3.2 CMOS input : Program Input (Prog)

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDD5V	5	V	
High level input voltage	V_{PROG}	See "programming conditions"		V	During programming
Low level input voltage	V_{IL}		0.3 * VDD5V	V	
Pull-down high level input current	I_{iL}		100	µA	VDD5V: 5.5V

19.3.3 CMOS Output Open Drain: MagRngn

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA	VDD5V: 4.5V VDD5V: 3V
Open drain leakage current	I_{OZ}		1	µA	

19.3.4 Tristate CMOS Output: DO

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	V_{OH}	VDD5V –0.5		V	
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA mA	VDD5V: 4.5V VDD5V: 3V
Tri-state leakage current	I_{OZ}		1	µA	

19.3.5 Digital-to-Analog Converter

Parameter	Symbol	Min	Typ	Max	Unit	Note	OTP setting
Resolution			10		bit		
Output Range	V_{OUTM1}	0		Vref	V	0……100% V_{ref} (default)	ClampMdEn = 0 (default)
	V_{OUTM2}	0.10 *V_{ref}		0.90 *Vref	V	10…..90% V_{ref}	ClampMdEn = 1
Output resistance	$R_{Out,DAC}$			8	kΩ	Unbuffered Pin DACout (#10)	
DAC reference voltage (DAC full scale range)	V_{ref}	0.2		VDD3V3 - 0.2	V	DAC reference = external: Pin: DACref (#9)	RefExt EN = 1
				VDD5V / 2	V	DAC reference = internal	RefExtEn = 0 (default)
Integral Non-Linearity	INL_{DAC}			+/- 1.5	LSB	Non-Linearity of DAC and OPAMP; -40….+125°C, For all analog modes: 1LSB = Vref / 1024	
Differential Non-Linearity	DNL_{DAC}			+/- 0.5	LSB		
Analog output hysteresis	Hyst			1	LSB	All analog modes	
				2	LSB	At 360°-0° transition, 360° mode only	OR1,OR0 = 00 (default)

19.3.6 OPAMP output stage

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Range	VDD5V	3.0		5.5	V	
Parallel Load Capacitance	CL			100	pF	
Parallel Load Resistance	RL	4.7			kΩ	3.3V operation
Open Loop Gain	A0	92	130	144	dB	
Offset Voltage RTI	VosOP	-5		5	mV	3 sigma
Output Range Low	VoutL			0.05 * VDD5V	V	Linear range of analog output
Output Range High	VoutH	0.95 * VDD5V			V	
current capability sink	Isink	4.8		50	mA	Permanent short circuit current: V_{out} to VDD5V
current capability source	Isource	4.6		66	mA	Permanent short circuit current: V_{out} to VSS
Output noise	V_{noise}	160	220	490	µVrms	Over full temperature range; BW= 1Hz...10MHz,Gain = 2x
OPAMP gain (non-inverting)	Gain		2			Internal; OTP: FB_int EN = 1
		1		4		External OTP: FB_int EN = 0 (default) With external resistors, pins Vout [#12] and FB [#11]: see Figure 14

19.4 Magnetic Input Specification

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Two-pole cylindrical diametrically magnetised source:

Parameter	Symbol	Min	Typ	Max	Unit	Note
Diameter	d_{mag}	4	6		mm	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets
Thickness	t_{mag}	2.5			mm	
Magnetic input field amplitude	B_{pk}	45		75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
Magnetic offset	B_{off}			± 10	mT	Constant magnetic stray field
Field non-linearity				5	%	Including offset gradient
Input frequency (rotational speed of magnet)	f_{mag_abs}			10	Hz	Absolute mode: 600 rpm @ readout of 1024 positions (see table 6)
	f_{mag_inc}			166	Hz	Incremental mode: no missing pulses at rotational speeds of up to 10,000 rpm (see table 6)
Displacement radius	Disp			0.25	mm	Max. offset between defined device center and magnet axis
Recommended magnet material and temperature drift			-0.12		%/K	NdFeB (Neodymium Iron Boron)
			-0.035			SmCo (Samarium Cobalt)

19.5 Electrical System Specifications

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution*	RES			10	bit	0.352 deg
Integral non-linearity (optimum) *	INL_{opt}			± 0.5	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement, T_{amb} =25 °C.
Integral non-linearity (optimum) *	INL_{temp}			± 0.9	deg	Maximum error with respect to the best line fit. Verified at optimum magnet placement , T_{amb} = -40 to +125°C
Integral non-linearity*	INL			± 1.4	deg	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, T_{amb} = -40 to +125°C
Differential non-linearity*	DNL			± 0.176	deg	10bit, no missing codes
Transition noise*	TN			0.06	Deg RMS	1 sigma, fast mode (pin MODE = 1)
				0.03		1 sigma, slow mode (pin MODE=0 or open)
Power-on reset thresholds						
On voltage; 300mV typ. hysteresis	V_{on}	1,37	2.2	2.9	V	DC supply voltage 3.3V (VDD3V3)
Off voltage; 300mV typ. hysteresis	V_{off}	1.08	1.9	2.6	V	DC supply voltage 3.3V (VDD3V3)
Power-up time, Until offset compensation finished, OCF = 1, Angular Data valid	t_{PwrUp}			20	ms	fast mode (pin MODE=1)
				80		slow mode (pin MODE=0 or open)
System propagation delay absolute output : delay of ADC and DSP	t_{delay}			96	µs	fast mode (pin MODE=1)
				384		slow mode (pin MODE=0 or open)
Internal sampling rate for absolute output:	$f_{S,mode0}$	2.48	2.61	2.74	kHz	T_{amb} = 25°C, slow mode (pin MODE=0 or open)
		2.35	2.61	2.87		T_{amb} = -40 to +125°C, slow mode (pin MODE=0 or open)
Internal sampling rate for absolute output	$f_{S,mode1}$	9.90	10.42	10.94	kHz	T_{amb} = 25°C, fast mode (pin MODE = 1)
		9.38	10.42	11.46		T_{amb} = -40 to +125°C, : fast mode (pin MODE = 1)
Read-out frequency	CLK	>0		1	MHz	Max. clock frequency to read out serial data

*)digital interface

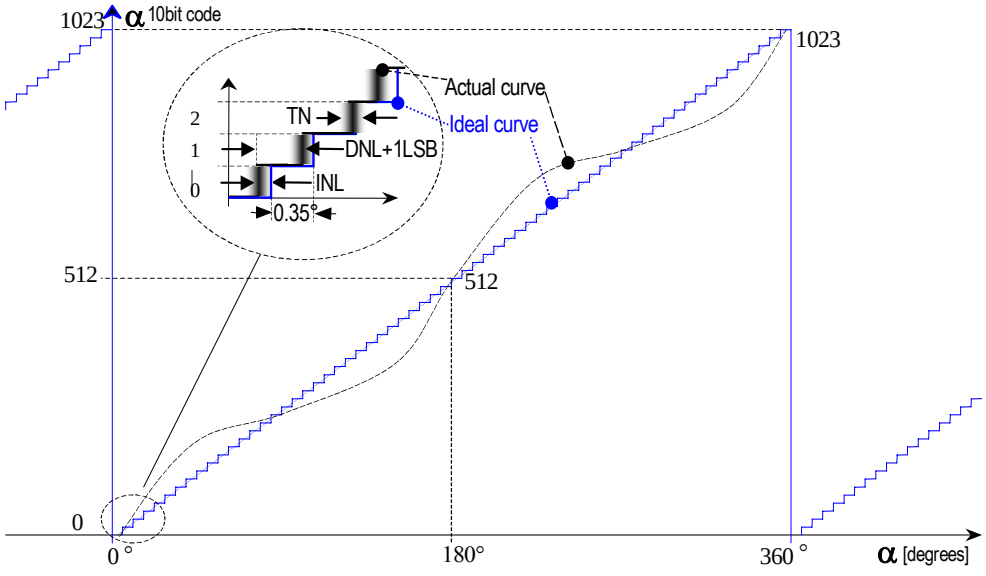


Figure 24: Integral and differential Non-Linearity (exaggerated curve)

Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

19.6 Timing Characteristics

Synchronous Serial Interface (SSI)

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data output activated (logic high)	t_{DO} active			100	ns	Time between falling edge of CSn and data output activated
First data shifted to output register	$t_{CLK\ FE}$	500			ns	Time between falling edge of CSn and first falling edge of CLK
Start of data output	$T_{CLK/2}$	500			ns	Rising edge of CLK shifts out one bit at a time
Data output valid	$t_{DO\ valid}$	357	375	394	ns	Time between rising edge of CLK and data output valid
Data output tristate	$t_{DO\ tristate}$			100	ns	After the last bit DO changes back to “tristate”
Pulse width of CSn	t_{CSn}	500			ns	CSn = high; To initiate read-out of next angular position
Read-out frequency	f_{CLK}	>0		1	MHz	Clock frequency to read out serial data

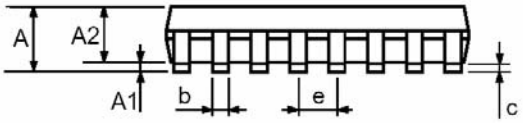
19.7 Programming Conditions

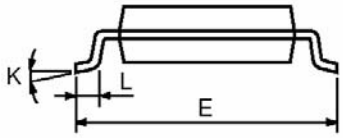
(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

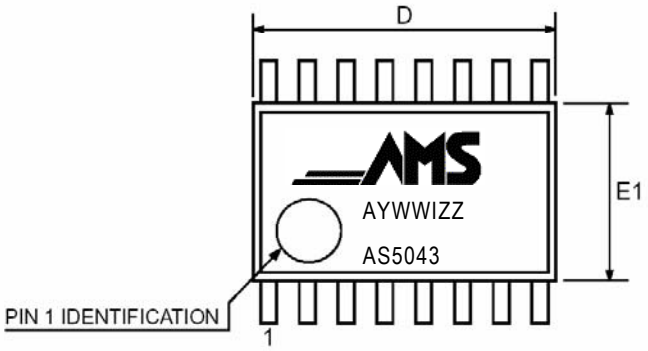
Parameter	Symbol	Min	Typ	Max	Unit	Note
Programming enable time	$t_{Prog\ enable}$	2			µs	Time between rising edge at Prog pin and rising edge of CSn
Write data start	$t_{Data\ in}$	2			µs	
Write data valid	$t_{Data\ in\ valid}$	250			ns	Write data at the rising edge of CLK_{PROG}
Load programming data	$t_{Load\ PROG}$	3			µs	
Rise time of V_{PROG} before CLK_{PROG}	t_{PrgR}	0			µs	
Hold time of V_{PROG} after CLK_{PROG}	t_{PrgH}	0		5	µs	
Write data – programming CLK_{PROG}	CLK_{PROG}			250	kHz	
CLK pulse width	t_{PROG}	1.8	2	2.2	µs	During programming; 16 clock cycles
Hold time of Vprog after programming	$t_{PROG\ finished}$	2			µs	Programmed data is available after next power-on
Programming voltage	V_{PROG}	7.3	7.4	7.5	V	Must be switched off after zapping
Programming voltage off level	$V_{ProgOff}$	0		1	V	Line must be discharged to this level
Programming current	I_{PROG}			130	mA	During programming
Analog read CLK	CLK_{Aread}			100	kHz	Analog readback mode
Programmed zener voltage (log.1)	$V_{programmed}$			100	mV	V_{Ref}-V_{PROG} during analog readback mode (see 13)
Unprogrammed zener voltage (log. 0)	$V_{unprogrammed}$	1			V	

20 Package Drawings and Markings

16-Lead Shrink Small Outline Package SSOP-16







Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.73	1.86	1.99	.068	.073	.078
A1	0.05	0.13	0.21	.002	.005	.008
A2	1.68	1.73	1.78	.066	.068	.070
b	0.25	0.315	0.38	.010	.012	.015
c	0.09	-	0.20	.004	-	.008
D	6.07	6.20	6.33	.239	.244	.249
E	7.65	7.8	7.9	.301	.307	.311
E1	5.2	5.3	5.38	.205	.209	.212
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.63	0.75	0.95	.025	.030	.037

1.1.1 Marking: AYWWIZZ

A: Pb-Free Identifier

Y: Last Digit of Manufacturing Year

WW: Manufacturing Week

I: Plant Identifier

ZZ: Traceability Code

JEDEC Package Outline Standard:

MO - 150 AC

Thermal Resistance $R_{th(j-a)}$:

typ. 151 K/W in still air, soldered on PCB

IC's marked with a white dot or the letters "ES" denote Engineering samples

21 Packing Options

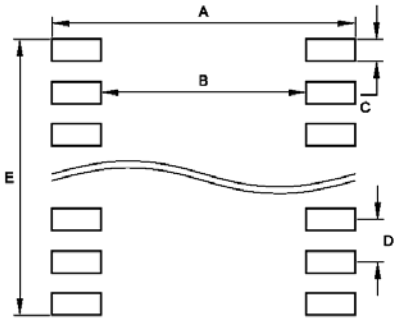
Delivery: Tape and Reel (1 reel = 2000 devices)

Tubes (1 box = 100 tubes á 77 devices)

Order # AS5043ASSU for delivery in tubes

Order # AS5043ASST for delivery in tape and reel

22 Recommended PCB Footprint:



Recommended Footprint Data		
	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

23 Revision History

Revision	Date	Description
1.6	Oct.3, 2006	Update DAC parameters (19.3.5), definition of magnet thickness
1.5	Aug.14, 2006	Update I_{supp} (19.2), B_{off} (19.4), $t_{DOvalid}$ (19.6), Ordering options (21)
1.4	Apr. 04, 2006	Update Programming Sequence Figure 11; Update Prog. Conditions 19.7 Include new OTP feature: permanent enabling of analog output (see 11.1.2).
1.3	Sep. 27, 2005	Update added features for Date Codes A534xx and higher: 10%/90% clamp levels, def. OPAMP gain = ext., r/y/g Field indicators, exit alignment mode by s/w, falling edge on analog response curve on 45° and 90° modes, jitter-free transition 360°/0° in analog mode. Update prop. delay and R_{th} of IC package
1.2	April 11, 2005	Add description for Analog modes and Programming
1.1	Feb. 18.2005	Update pin assignment and operating modes
1.0	Dec. 7, 2004	initial revision

24 Contact

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